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EFFICIENT FFT/IFFT IMPLEMENTATION TECHNIQUE OF OFDM ON FPGA

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ABSTRACT: Orthogonal Frequency Division Multiplexing (OFDM) is a multicarrier system which modulate and multiplex the data. It has been adopted by most wireless and wired communication standards. The idea is to utilize a number of carriers, spread regularly over a frequency band, in such a way so that the available bandwidth is utilized to maximal efficiency. IFFT/ FFT blocks are complex to implement and main blocks of OFDM system i.e. it consumes more resources. So, a efficient technique used here in which FFT/IFFT is implemented in such a way that it consumes very less resources. In this paper the design and implementation of OFDM on a Field Programmable Gate Array (FPGA) device has been presented. The implementation was made on FPGA allows flexibility in design and also it can achieve higher computing speed than digital signal processors. ASIC-like performance with lower development time and risks can also be achieved.

Keywords: FFT, IFFT, OFDM, carrier signal, orthogonal

1. INTRODUCTION

Orthogonal Frequency Division Multiplexing is a special case of multicarrier transmission, where a single data stream is transmitted over a number of lower-rate subcarriers. The main advantage of OFDM is their robustness to channel fading in wireless environment. OFDM can be seen as either a modulation technique or a multiplexing technique. In OFDM, multiplexing is applied to independent signals but these independent signals are the part of one main signal. In OFDM, the signal itself is first split into independent channels, modulated by data and then re-multiplexed to create the OFDM carrier [1].OFDM is a technique especially suitable for wireless communication due to its resistance to inter-symbol interference (ISI) and inter-carrier interference(ICI). In single carrier system, if signal get fade or interfered then entire link gets failed where as in multicarrier system, only a small percentage of the subcarriers will be affected.FFT/IFFT are the complex and important block of OFDM system, it also requires much of the resources. So its efficient implementation regarding power and resources is must. So in this paper for implementation of FFT, very efficient and innovative technique is proposedby Koushik Maharatna, Eckhard Grass, and Ulrich Jagdhold [2] is used.

II. OFDMA SYSTEM

Mathematically modulating a waveform and adding it is equivalent to taking an IFFT. This is because the time domain representation of OFDM is made up of different orthogonal sinusoidal signals which are nothing but inverse Fourier transform. The block diagram of digital OFDM system is shown in Fig 1. Since the OFDM signal is in time domain, IFFT is the appropriate choice to use in the transmitter, which can be thought of as converting frequency domain samples to time domain samples. Fig. 1 illustrates how the use of IFFT in

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the transmitter eliminates the need for separate sinusoidal converters. IFFT and FFT blocks in the transmitter are interchangeable as long as their duals are used in receiver[3,4].

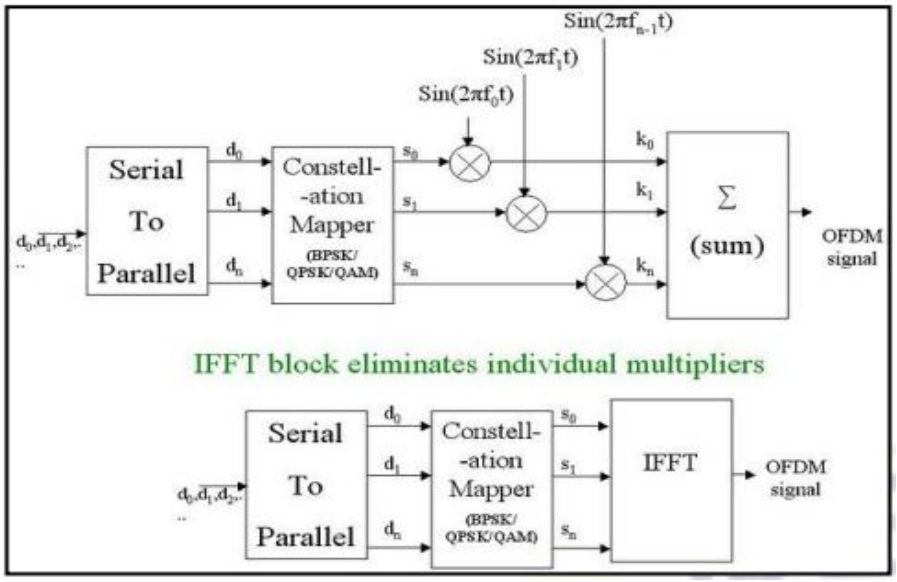

FIG 1 OFDM implementation using FFT/IFFT

III. EXISTING SYSTEM

The input data stream is split into N parallel low bandwidth modulated data streams. Due to orthogonality of subcarriers they do not interfere with one another. Each subcarrier has a low symbol rate. But the combination of subcarriers carrying the information in parallel allows for high data rates. Low symbol rate is used to reduce the problem of Inter Symbol Interference (ISI) [5,6]. Before modulation the transmitter stage of an OFDM transceiver takes data, Converts the data and encodes it into a serial stream. The generation of OFDM signal is takes place by using Inverse Fast Fourier Transform (IFFT). Reverse process takes place in receiver stage.

The block diagram of existing system[7] is explained briefly .The BPSK Modulation scheme is one of the Phase shift keying Technique that can be used for the Modulation, with 180 phase shift keying is applied. The Serial to parallel block contains Technique that converts serial form input data to parallel form outputs, it converts the data serial inputs to parallel outputs that can be works after getting all inputs in the parallel signal. The IFFT Block is converts the Input data from Frequency domain to Time domain outputs. The Cyclic Prefix is block that assigns empty memory space with your input data in the base of 1/N value of the input is to be assigned for cyclic prefix memory. The Receiver block contains Remove cyclic prefix block, serial to parallel block, FFT Block, Parallel to serial block, Demodulation. The Remove cyclic prefix is removes the empty space that created in the transmitter block. The cyclic prefix Memory is contains noise and errors that can be removed in this block. The Fast Fourier Transform block is performs the input from time to frequency operations. The FFT blocks basically contains different type of radix based FFT architectures such as Radix-2 , Radix-4, Mixed- Radix • and Split Radix. we propose the pipelined implementation of Radix-2 based single delay feedback (R2SDF), Radix-2 single delay commutator (R2SDC), combined architecture is implemented in the receiver architecture of OFDM.

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III PROPOSED SYSTEM

The proposed FFT architecture(fig.2) consists of one pre-stage, log2N-1 SDC stages, one post-stage, one SDF stage, and one bit reverser, The pre-stage shuffles the Complex input data to a new sequence that consists of real part followed by the corresponding imaginary part, shown in Table 1. The corresponding post-stage shuffles back the new sequence to the complex format. The SDC stage t (t = 1, 2, .., log2N − 1) contains a SDC PE, which can achieve 100% arithmetic resource utilization of both complex adders and complex multipliers. Final, the even data are retrieved in normal order. Thus, the bit reverser requires only N/2 data buffer. The last stage of Single Delay Feedback (SDF) is identical to the radix-2 Single Delay Feedback (SDF), containing a complex adder and a complex subtractor. By using the modified addressing method12, the data with an even index are written into memory in normal order, and they are then retrieved from memory in bit-reversed order while the ones with an odd index are written in bitreversed order. Normally the Fast Fourier Transform architectures are working based upon the parallel architectures, so FFT's are consume large area and latency, in order to perform low area and latency we are in deed in developing the pruning the FFT's with help of Pipelining Data path, feed forward, feed backward. And some various architectures for reducing the area and delay of the FFT processors, there are various radix-2 based architectures such as R2MDC, R2SDF, R2SDC; these architectures are very useful in making the pipelined operation of FFT's

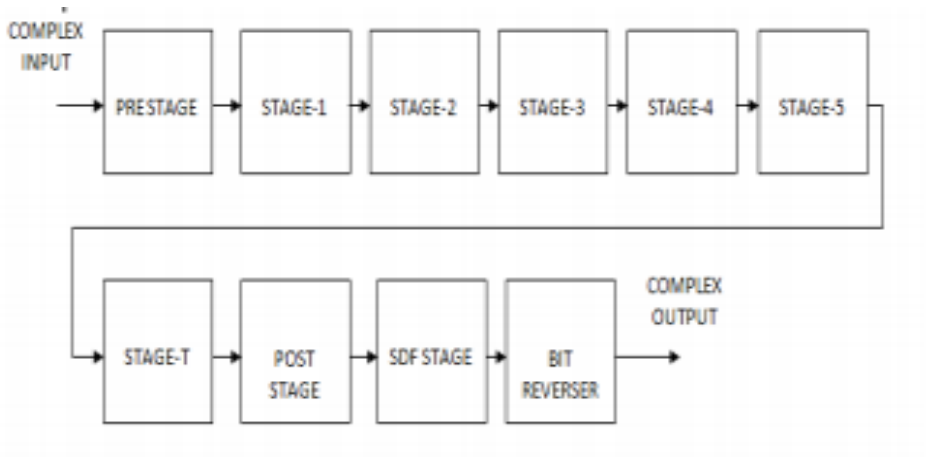

Fig 2 Proposed system

The proposed system consists of the architecture that can be have the stage-1, stage-2, stage-3, stage-4, stage-5 all are designed for 64-point FFT architectures, as shown in the Figure 2. The proposed system consists of five stages and the stage-t which is also present in 64-point FFT architecture, All FFT based architectures are Operating based upon the parallel architectures, so we are proposing a Pipelined operation of FFT radix-2 architectures with combination of SDF-SDC architectures in order to achieve higher data rate.

IV RESULTS and DISCUSSION

The proposed system is implemented in Xilinx based Spartan- 3e FPGA. The codings were written in Hardware Description Language(VHDL) and synthesized in xilinix ISE 10.1 and simulated using model sim simulator.

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	AREA (SLICE UTILIZATION)	LUT	DELAY (NS)	FREQUENCY (MHZ)	POWER (W)
EXISTING[7]	1062	563	4.21	246.95	2.83
PROPOSED	875	799	7.56	67.79	0.29

Table 1. Comparision of OFDM systems

In our proposed system the though delay get increased compared to existing system, the power has been reduced to 60%. Thus our proposed system is more suitable for low power VLSI applications.

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